THÔNG TIN LUẬN ÁN

Tên luận án : **Nghiên cứu Null Convention Logic trong thiết kế vi mạch bất đồng bộ**
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ABSTRACT

For decades, the synchronous designs have played an important role in the digital circuit systems. However, as the technology develops, electronic devices also require higher requirements such as the processing speed must be faster, the chip size must be smaller, and power consumption must be lower to maintain a battery for a long time. As a result, the synchronous circuits are very difficult to meet the requirements mentioned above because of the clock related problems, including clock skew, glitch, electromagnetic interference, the layout of the clock distribution network, especially the power reduction. In contrast, the asynchronous integrated circuits do not use clocks, so it could overcome some of the disadvantages related to clocks as mentioned above. Therefore, in this dissertation, the author focuses on the following three issues:

- The first is to study the asynchronous circuit design method based on Null Convention Logic (NCL).

- The second is to study the conversion flow from the synchronous design to the NCL-based asynchronous design.

- The third is to study to improve the standard cell library design flow and propose to design two sets of static and semi-static NCL cell libraries for the synthesis of the asynchronous designs.

Researching on the NCL-based asynchronous circuit design method, the author has systematized some problems related to NCL-based circuit design. The asynchronous circuits designed based on NCL use the local handshake protocol to synchronize their operations, so components in the circuit only perform switching when needed, this feature is unlike in the synchronous circuit. Therefore, the switching power in asynchronous circuits designed based on NCL is significantly reduced compared to synchronous circuits. To illustrate the method mentioned above, and its characteristics, the AES algorithm is chosen as an illustrative example of the method. In addition to implementing the above example by the asynchronous method based on NCL, the above design is also implemented by the synchronous method in this dissertation. Both synchronous and NCL-based asynchronous designs are implemented on FPGA and simulated, tested with ASIC approach. From there as a basis for the comparison between the two methods on parameters such as power, area and speed. In addition, the power parameters of the asynchronous method are compared with the research results of other authors. Research results with ASIC approach have shown that the power consumption of the NCL-based asynchronous circuits could be improved by about 71% compared to the synchronous circuits. In addition, the research results on FPGA also give similar results, the power of the NCL-based asynchronous circuit also improves about 40% compared to the synchronous circuit.

The NCL-based asynchronous integrated circuit design method is not only suitable for the design of the low power integrated circuits, but also suitable for the design of security and data-safety circuits. Therefore, in order to improve the circuits designed by the synchronous method without having to redesign in order to save time and effort, choosing tools to convert from the synchronous design to the asynchronous design is necessary and also studied in this dissertation. Among many conversion tools, UNCLE is chosen to convert from the synchronous design to the asynchronous design based on NCL because of its advantages. In the UNCLE conversion flow, Verilog RTL code files are converted to a single rail netlist of D flip-flops, latches, and logic gates. This netlist is converted into a dual-rail asynchronous netlist and optimized by many other functions.

This netlist can then be synthesized using various tools. The Subbyte transformation that performs the S-box block in the AES encryption is performed to test the conversion flow. In addition, the converted netlist can be simulated using UNCLE's Unclesim.

In the synthesis process, most NCL-based asynchronous designs are synthesized using synchronous libraries. This is a great difficulty and disadvantage for those who study the asynchronous circuits, especially for the university students. To solve the problem of the lack of a cell library for the synthesis of the asynchronous designs, the author proposed to improve the standard cell library design flow and also proposed the design of NCL cell libraries for the asynchronous designs. Thanks to that flow, researchers can create their own cell libraries in different technologies and update new cells easily.

Based on the proposed cell library design flow, the semi-static and static NCL cell libraries are designed. The design flow of cells was implemented using Cadence Virtuoso and Synopsys Design Compiler. In this flow, cells are designed based on 45nm PDK and simulated for functional testing in various corners. In addition, Ocean script and EDA environment were used to improve the cell library design flow and to support the automatic cell characterization to extract the time and power models. These models are used to create .lib files. This file is converted to a .db file to create a library. The complete 27-cell NCL library is used to synthesize the NCL-based asynchronous designs. Besides, to compare the static and semi-static NCL cell libraries in this dissertation with the NCL cell libraries of other authors, the author has compared the synthesis results of the 4-bit full adder using the proposed NCL cell libraries and the NCL cell library of another author. The synthesis results have shown that the power consumption of the 4-bit full adder could be improved about 20% when synthesized by the static NCL cell library and about 39% when synthesized by the semi-static NCL cell library compared to the static NCL cell library of other authors.

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