VIETNAM NATIONAL UNIVERSITY
HO CHI MINH CITY
UNIVERSITY OF TECHNOLOGY

SOCIALIST REPUBLIC OF VIETNAM
Independence – Liberty – Happiness

DISSERTATION INFORMATION

Dissertation's title: **Studies and Design of Low-Density Parity-Check (LDPC) Decoders in New Generation Communication Systems.**

Major: **Electronics Engineering**. Major code: **9520203**.

PhD candidate: **Tran Thi Bich Ngoc**.

Scientific superviors: **1. Assoc. Prof. Dr. Hoang Trang.**

2. Dr. Nguyen Ly Thien Truong.

University: **Ho Chi Minh City University of Technology, Vietnam National University - Ho Chi Minh City.**

ABSTRACT

Error correction coding is crucial in digital communications and data storage systems, aiming to ensure the reliable transmission of information. Among the available error correction codes, Low-Density Parity-Check (LDPC) codes stand out as one of the most effective, capable of nearing the Shannon limit. Since their rediscovery in the mid-1990s, LDPC codes have attracted significant attention from both academia and industry. They are extensively applied across numerous communication standards and digital storage solutions due to their superior error correction capabilities, efficient hardware utilization, and high processing throughput. Specifically, LDPC codes have been selected for 5G new radio technologies, which demand enhanced processing speeds, the ability to handle large volumes of data, and minimal hardware resource consumption. However, the optimal solutions for LDPC decoders, as applied in previous scenarios, may fall short of 5G standards' demands, owing to the extensive code length, irregular patterns, significant storage needs, and heightened processing requirements. In this thesis, the author delve into three primary areas: Firstly, the author explore ways to enhance the decoding accuracy of the Min-Sum decoding algorithm. Secondly, the author examine the distinctive characteristics of the 5G LDPC code, proposing a method to reduce storage requirements. Lastly, the author design an LDPC decoder that employs various techniques to optimize hardware resource use and boost decoding efficiency.

The iterative Message-Passing algorithm, notably the Belief-Propagation (BP) algorithm, is pivotal in decoding LDPC codes, offering near-Shannon limit optimal decoding performance. Despite its effectiveness, the BP algorithm's computational intensity has prompted the development of the Min-Sum (MS) algorithm, which simplifies operations to comparisons and additions, thereby reducing computational complexity. Nonetheless, the MS algorithm's reliance on a minimum function within the Check Node (CN) process yields an approximate message, resulting in notable degradation of decoding performance in error correction.

In response to this challenge, this research has formulated several strategies to refine decoding accuracy using the Min-Sum algorithm, presenting mathematical evidence to bolster error correction capabilities. A principal strategy involves implementing correction factors to mitigate information overestimation inherent in the MS algorithm's approximation technique. This thesis introduces various adjustment methods for these correction factors, targeting check node processing improvements (via the Improved Offset Min-Sum (IOMS) and Advanced Offset Min-Sum (AOMS) algorithms) and simultaneous adjustments across variable node and check node processes (through the Variable Offset Min-Sum (VOMS), Hybrid Offset Min-Sum (HOMS), and Enhanced Single Minimum Min-Sum (EsmMS) algorithms).

The objective of this study is to craft effective algorithms for LDPC decoder design. Through simulations conducted in MATLAB R2022b, this research evaluates the decoding efficacy of the 5G LDPC code across multiple code rates (1/2, 2/3, 3/4, 3/5) and lengths (4080, 13056, 7424, 8832, 6720) utilizing the BG1 matrix. The findings reveal that the HOMS algorithm substantially improves decoding performance by 0.38 dB over the MS algorithm at a Bit Error Rate (BER) of 10^{-8}. Furthermore, the AOMS algorithm outperforms the Simplified Minimum Approximation Min-Sum (SMA-MSA) algorithm by 0.26 dB, showcasing the potential of these proposed enhancements in advancing error correction efficiency.

The design of FPGA-based decoders for LDPC codes is influenced by various system attributes, including processing throughput, hardware resource demands, and error correction effectiveness. This thesis introduces an FPGA hardware design for LDPC decoders tailored to 5G applications, incorporating the Hybrid Offset Min-Sum (HOMS) and Enhanced Single Minimum Min-Sum (EsmMS) algorithms as the core decoding mechanisms. To optimize hardware efficiency and improve decoding performance, the implementation employs several strategies: layered scheduling to enhance data flow, precise quantization bit selection to balance accuracy and resource usage, a partially parallel architecture to improve throughput while conserving resources, and varying levels of parallelism to adapt to specific hardware constraints. Unlike traditional Min-Sum (MS) decoders, which necessitate calculating the first two minimum values among all variable-to-check message inputs during the

check node process, the proposed design simplifies this requirement by determining only the first minimum value. This adjustment significantly reduces hardware complexity and associated costs, providing a more efficient and effective solution for LDPC decoding in next-generation communication systems.

The memory requirements for LDPC decoders, particularly in the context of 5G LDPC codes, are significantly influenced by the check node degree. Given the irregular nature of 5G codes, which results in substantial variation in check node degrees across different layers, utilizing a uniform maximum check node degree for design purposes can lead to excessive memory usage. To address this challenge, this thesis introduces a novel memory division strategy based on check node degree, effectively mitigating the issue of memory wastefulness.

The implementation of the proposed Hybrid Offset Min-Sum (HOMS) and Enhanced Single Minimum Min-Sum (EsmMS) decoders on the Xilinx Kintex UltraScale+ FPGA platform demonstrates their efficiency and performance. With 10 decoding iterations, these decoders achieve throughputs of up to 2.82 Gbps for a 5G LDPC code length of 8832 bits at a code rate of 1/2. Operating at maximum frequencies of approximately 142.8 MHz for the EsmMS decoder and 153.5 MHz for the HOMS decoder, they exhibit hardware usage efficiencies of 4.96 and 4.65 hardware resources/layer.Mbps, respectively. Remarkably, these efficiencies are 4.5 to 5 times superior to those of conventional reference decoders, underscoring the significant improvements in both performance and resource utilization brought about by the proposed design methodology.

Scientific superviors **PhD Candidate**

Assoc. Prof. Dr. Hoang Trang **Dr. Nguyen Ly Thien Truong** **Tran Thi Bich Ngoc**