VIETNAM NATIONAL UNIVERSITY
HO CHI MINH CITY
UNIVERSITY OF TECHNOLOGY

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DISSERTATION INFORMATION

Dissertation's title: **Study, design, simulate fabrication process of Floating-gate MOS transistor.**

Major: **Electronics Engineering** Major code: **9520203**

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ABSTRACT

Floating-gate MOS transistor has been receiving much attention in recent decades because it offers many essential benefits in the integrated circuit design field and offers many applications. In general, this MOS is a type of the conventional MOSFET where an additional floating gate is completely surrounded by dielectrics. Floating-gate MOS transistor has been used in many fields of analog mixed-signal applications, neural networks, especially in nonvolatile memories. It has also been investigated as a potential storage element in both analog and digital designs.

However, based on the industry demands, whereas the scaling down of the CMOS device improves the speed operation, power dissipation, and fabrication cost, there is a challenge about the limitation of the tunnel oxide layer thickness which is indicated by IRDS and Intel with the limit value of 6 nm. The challenge is that when the tunnel oxide layer thickness is extremely thin, the leakage of stored charges on the floating gate becomes dominant and leads to an increase the power dissipation and degrades the Floating-gate MOS transistor performances such as retention time, endurance, memory window, etc. Moreover, reducing the tunnel oxide layer thickness also decreases the gate capacitance ratio (GCR), which has to retain greater than 0.6. The GCR has a significant impact on the Write/Erase and Read operating speeds of the device. The low GCR leads to poor gate control and requires higher operation voltage to compensate for the low capacitance. Therefore,

finding the solutions to solve the challenge as stated above in tunnel oxide layer thickness plays a pivotal role in the development of the integrated circuit design field.

In solving the challenge, many studies have been published over the past decades. Overall, there are three main types of approaches. While the first approach proposes the new structures of Floating-gate MOS transistor, the second approach investigates the new materials for the fabrication process, and the third approach mainly focuses on optimization for the existing standard Floating-gate MOS transistor.

In this work, to overcome these problems in memory window, speed, leakage power, and tunnel oxide layer thickness, the Nanocrystal Floating-gate MOS transistor was investigated in the first approach, and the standard Floating-gate MOS transistor was taken into account in the third one. This work proposed two sets of structure parameters in virtual fabrication for the devices in the two approaches which provide good device performances and overcome the problems. Especially, the performance of the Nanocrystal Floating-gate MOS transistor has been significantly improved, such as 2.8 V of the memory window with the supply voltage of ±6 V at the control gate, and the rapid erasing speeds of 2.03 μs, 28.6 ns, and 1.6 ns when the low control gate voltages are ±9 V, ±12 V, and ±15 V, respectively. Besides, the standard Floating-gate MOS transistor can achieve 4 V of the memory window with the supply voltage of ±6 V, and erasing speeds of 1 μs, 15 ns, and 0.9 ns when the low control gate voltages are ±9 V, ±12 V, and ±15 V.

Furthermore, this work aims to propose a methodology of virtual fabrication for semiconductor devices and design a tool called Technology Computer-Aided Design Automatic Simulation (TCADAS) which can perform a completely virtual fabrication, device simulation, process variation, and output extraction. Especially, the TCADAS tool eliminates drudgery when studying semiconductor devices such as complexity in setting inputs, substantial manual work, and long run time of simulations. The Nanocrystal MOS transistor and the standard Floating-gate MOS transistor, which are mentioned above, were studied and investigated by the use of the designed TCADAS tool.

Next, after designing the expected standard Floating-gate MOS transistor, this work aims to do an extraction DC model for the device in order to apply it in real applications such as nonvolatile memories. There are two methods which were adopted in this work. First, with a simple approach, this work proposed the use of a standard industrial ICCAP tool in investigating and extracting the DC model where the Level 3 model is deployed. Second, the combination architecture of the MOS transistor, capacitance, and voltage-controlled voltage source was applied in order to achieve a high accuracy result and solve the accuracy limitation of the first method. In this work, the industrial standard model Berkeley Short-channel IGFET Model (BSIM) 3v3.1, level 49 was deployed, and the DC simulation was obtained with the use of the LTspice tool.

Finally, in order to perform validation of the results of the standard Floating-gate MOS transistor which was the extracted DC models including Level 3 and BSIM3v3.1 level 49 models, these results were compared to a real fabrication on silicon of a standard Floating-gate MOS in industry. Regarding the comparison results, while the data of the BSIM3v3.1 level 49 model are reasonable, the accuracy of the Level 3 model is as expected as the limitation of the particular version.

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